

CLAIMS

What is claimed is

1 1. A crossbar device comprising:

2 n input lines;

3 m output lines; and

4 a plurality of chains of pass transistors, each having a plurality of pass

5 transistors, to selectively couple said n input lines to said m output lines;

6 where n and m are integers.

1 2. The crossbar device of claim 1, wherein at least one of the plurality of chains of

2 pass transistors consists of a first and a second pass transistor.

1 3. The crossbar device of claim 1, wherein each of the plurality of chains of pass

2 transistors consists of a first and a second pass transistor.

1 4. The crossbar device of claim 1, wherein the device further comprises a plurality of

2 memory elements coupled to the input lines.

1 5. The crossbar device of claim 1, wherein the device further comprises a plurality p

2 to q decoder logic coupled to the input lines, where p and q are integers, with p

3 being less than q.

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1 6. The crossbar device of claim 1, wherein each of said chains of pass transistors
2 further comprises a memory element coupled to a pass transistor of the chain,
3 disposed on an input side of the chain to control the chain.

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1 7. A reconfigurable circuit comprising:
2 a plurality of crossbar devices coupled to one another, each crossbar device
3 having at least a memory element, and an output buffer electrically associated with
4 the memory element; and
5 a voltage supply structure coupled to the crossbar device designed to supply
6 Vdd to the output buffers, and a voltage raised by a threshold over Vdd to the
7 memory elements to maintain the input voltage of the output buffers at Vdd.

1 8. The reconfigurable circuit of claim 7, wherein at least one of the plurality of
2 crossbar devices comprises
3 n input line;
4 m output lines; and
5 a plurality of chains of pass transistors coupling the n input lines to the m
6 output lines;
7 where n and m are integers.

1 9. The reconfigurable circuit of claim 8, wherein at least one of the plurality of chains
2 of pass transistors consists of a first and a second pass transistor.

1 10. The reconfigurable circuit of claim 8, wherein each of the plurality of chains of
2 pass transistors consists of a first and a second pass transistor.

1 11. The reconfigurable circuit of claim 7, wherein each of the plurality of crossbar
2 devices comprises
3 n input line;
4 m output lines; and
5 a plurality of chains of pass transistors coupling the n input lines to the m
6 output lines;
7 where n and m are integers.

1 12. The crossbar device of claim 11, wherein each of said chains of pass transistors
2 further comprises a memory element coupled to a pass transistor of the chain,
3 disposed on an input side of the chain to control the chain.

1 13. The reconfigurable circuit of claim 7, wherein the reconfigurable circuit is an
2 integrated circuit.

1 14. The reconfigurable circuit of claim 7, wherein the reconfigurable circuit is a block
2 of an integrated circuit.

1 15. A reconfigurable circuit comprising:
2 a plurality of crossbar devices coupled to one another, each crossbar device
3 having at least an output buffer; and
4 a power-on circuitry coupled to the crossbar devices to force the output
5 buffers to a known state at power-on.

1 16. The reconfigurable circuit of claim 15, wherein the power-on circuitry comprises
2 a flip-flop.

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1 17. The reconfigurable circuit of claim 15, wherein at least one of the plurality of
2 crossbar devices comprises
3 n input line;
4 m output lines; and
5 a plurality of chains of pass transistors coupling the n input lines to the m
6 output lines;
7 where n and m are integers.

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1 18. The reconfigurable circuit of claim 17, wherein at least one of the plurality of
2 chains of pass transistors consists of a first and a second pass transistor.

1 19. The reconfigurable circuit of claim 17, wherein each of the plurality of chains of
2 pass transistors consists of a first and a second pass transistor.

1 20. The reconfigurable circuit of claim 15, wherein each of the plurality of crossbar
2 devices comprises
3 n input line;
4 m output lines; and
5 a plurality of chains of pass transistors coupling the n input lines to the m
6 output lines;
7 where n and m are integers.

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1 21. The crossbar device of claim 20, wherein each of said chains of pass transistors
2 further comprises a memory element coupled to a pass transistor of the chain,
3 disposed on an input side of the chain to control the chain.

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1 22. The reconfigurable circuit of claim 15, wherein
2 each crossbar device further having at least a memory element electrically
3 associated to an output buffer; and
4 the reconfigurable circuit further comprises a voltage supply structure
5 coupled to the crossbar devices designed to supply Vdd to the output buffers, and a
6 voltage raised by a threshold over Vdd to the memory elements to maintain the
7 voltage supply of the output buffers at Vdd.

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1 23. The reconfigurable circuit of claim 15, wherein the reconfigurable circuit is an
2 integrated circuit.

1 24. The reconfigurable circuit of claim 15, wherein the reconfigurable circuit is a
2 block of an integrated circuit.